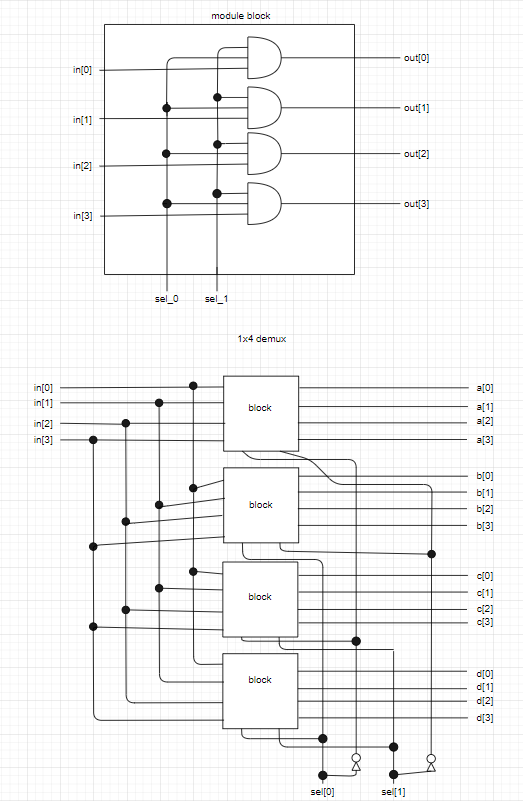
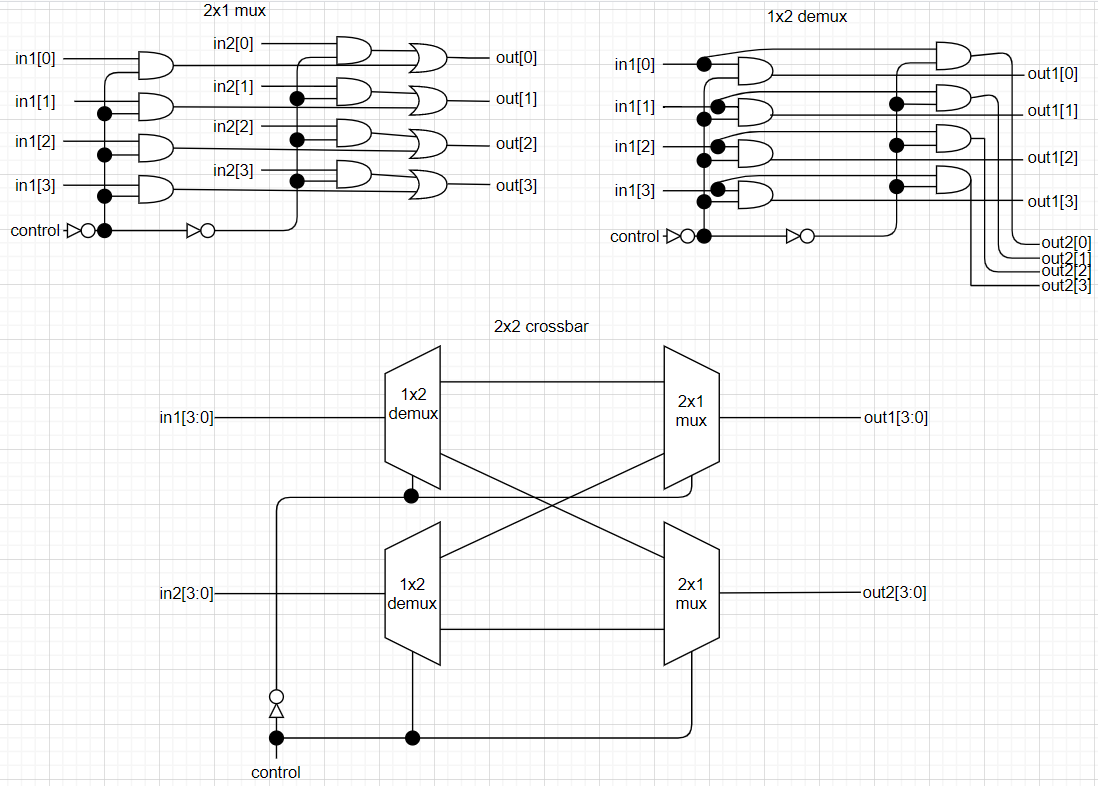
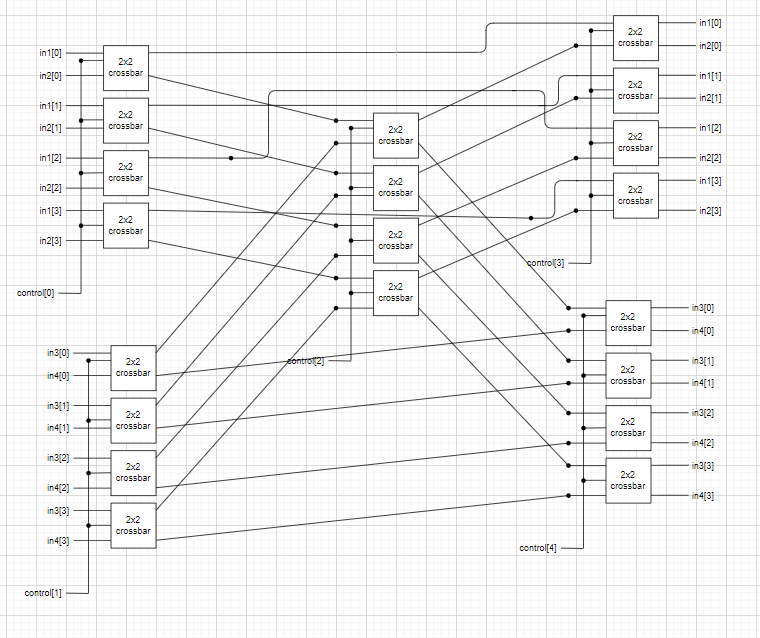
3. 4-bit 4x4crossbar with simple crossbar switch

According to the second question, we can write the code based on the graph.

We just follow the graph.







How do we test our module?

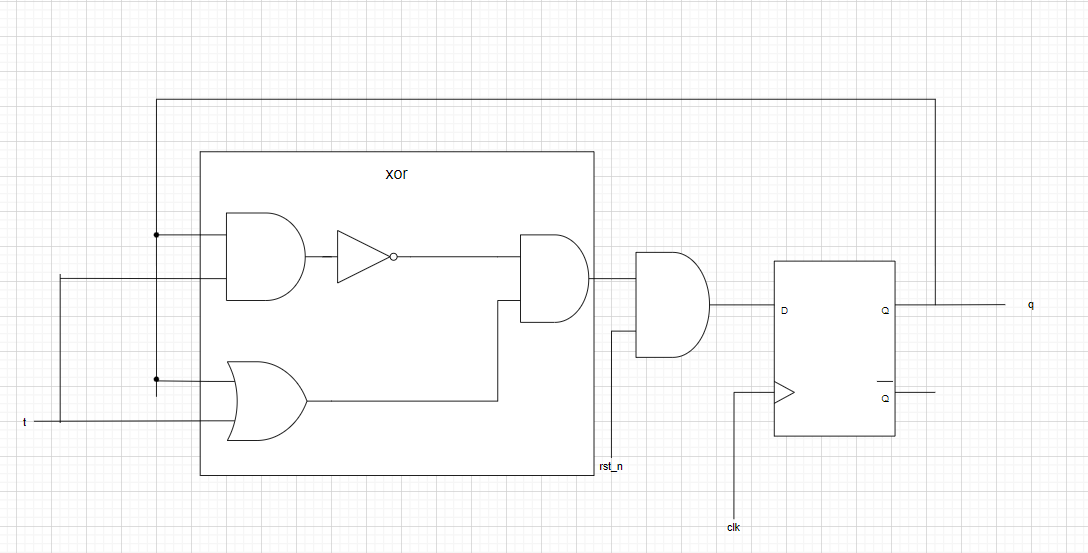
4.

We know that a t-flip-flop will change the output if t is 1. So we use a xor gate to implement. If t equals 1 and q equals 1, the output is 0 after go through xor gate.

How do we implement a xor gate? We use a truth table to find it.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | A+B | AB | (AB)’ | (A+B)(AB)’ |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

With the graph of t-flip-flop, we can build the module easily.



How to test our module?

We refer to the D-flip-flop’s testbench. Every negative edge we let t’s value change.

Thus we can determine whether it is right by the graph.

Contributions:

徐嘉徽做1.2題

李佳栩做3.4題

一起研究fpga的那題。

Actually, We are not familiar with Verilog. We often use wrong thoughts like the way we practice C++. So it is hard for us to learn a hardware language. After some practices, we finally have a deeper understandings of Verilog. Look forward to the next assignment.